Quad Single Supply Comparators

These comparators are designed for use in level detection, low-level sensing and memory applications in consumer, automotive, and industrial electronic applications.

- Single or Split Supply Operation
- Low Input Bias Current: 25 nA (Typ)
- Low Input Offset Current: ±5.0 nA (Typ)
- Low Input Offset Voltage
- Input Common Mode Voltage Range to Gnd
- Low Output Saturation Voltage: 130 mV (Typ) @ 4.0 mA
- TTL and CMOS Compatible
- ESD Clamps on the Inputs Increase Reliability without Affecting Device Operation

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}		Vdc
LM239/LM339/LM2901, V		+36 or ±18	
MC3302		+30 or ±15	
Input Differential Voltage Range	V_{IDR}		Vdc
LM239/LM339/LM2901, V		36	
MC3302		30	
Input Common Mode Voltage Range	V _{ICMR}	-0.3 to V _{CC}	Vdc
Output Short Circuit to Ground (Note 1.)	I _{SC}	Continuous	
Power Dissipation @ T _A = 25°C	P _D		
Plastic Package		1.0	W
Derate above 25°C		8.0	mW/°C
Junction Temperature	TJ	150	°C
Operating Ambient Temperature Range	T _A		°C
LM239		-25 to +85	
MC3302		-40 to +85	
LM2901		-40 to +105	
LM2901V		-40 to +125	
LM339		0 to +70	
Storage Temperature Range	T _{stg}	-65 to +150	°C

The maximum output current may be as high as 20 mA, independent of the magnitude of V_{CC}. Output short circuits to V_{CC} can cause excessive heating and eventual destruction.

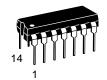


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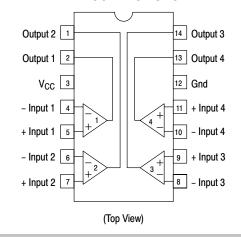


SO-14 D SUFFIX CASE 751A



PDIP-14 N, P SUFFIX CASE 646

PIN CONNECTIONS

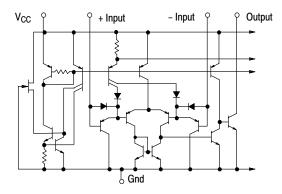


ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 6 of this data sheet.



NOTE: Diagram shown is for 1 comparator.

Figure 1. Circuit Schematic

ELECTRICAL CHARACTERISTICS ($V_{CC} = +5.0 \text{ Vdc}$, $T_A = +25 ^{\circ}\text{C}$, unless otherwise noted)

		LM239/339 LM2901/2901V				MC3302					
Characteristic	Symbol	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
Input Offset Voltage (Note 3.)	V _{IO}	-	±2.0	±5.0	_	±2.0	±7.0	-	±3.0	±20	mVdc
Input Bias Current (Notes 3., 4.) (Output in Analog Range)	I _{IB}	-	25	250	-	25	250	-	25	500	nA
Input Offset Current (Note 3.)	I _{IO}	-	±5.0	±50	-	±5.0	±50	-	±3.0	±100	nA
Input Common Mode Voltage Range	V _{ICMR}	0	-	V _{CC} -1.5	0	-	V _{CC} -1.5	0	-	V _{CC} -1.5	V
Supply Current $R_L = \infty$ (For All Comparators) $R_L = \infty$, $V_{CC} = 30 \text{ Vdc}$	Icc	1 1	0.8 1.0	2.0 2.5	_ _	0.8 1.0	2.0 2.5	1 1	0.8 1.0	2.0 2.5	mA
Voltage Gain $R_L \ge 15 \text{ k}\Omega$, $V_{CC} = 15 \text{ Vdc}$	A _{VOL}	50	200	-	25	100	-	25	100	-	V/mV
Large Signal Response Time $\begin{aligned} &V_{l} = \text{TTL Logic Swing,} \\ &V_{ref} = 1.4 \text{ Vdc, } V_{RL} = 5.0 \text{ Vdc,} \\ &R_{L} = 5.1 \text{ k}\Omega \end{aligned}$	_	-	300	-	-	300	-	-	300	_	ns
Response Time (Note 5.) $V_{RL} = 5.0 \text{ Vdc}, R_L = 5.1 \text{ k}\Omega$	1	ı	1.3	ı	-	1.3	-	I	1.3	-	μs
Output Sink Current $V_{I}(-) \ge +1.0 \text{ Vdc}, V_{I}(+) = 0,$ $V_{O} \le 1.5 \text{ Vdc}$	I _{Sink}	6.0	16	-	6.0	16	-	6.0	16	_	mA
Saturation Voltage $V_I(-) \ge +1.0 \text{ Vdc}, V_I(+) = 0,$ $I_{sink} \le 4.0 \text{ mA}$	V _{sat}	_	130	400	_	130	400	_	130	500	mV
Output Leakage Current $V_I(+) \ge +1.0 \text{ Vdc}, V_I(-) = 0,$ $V_O = +5.0 \text{ Vdc}$	I _{OL}	-	0.1	-	-	0.1	_	_	0.1	-	nA

 $[\]begin{array}{ll} \text{2.} & (\text{LM239}) \ \text{T}_{\text{low}} = -25^{\circ}\text{C}, \ \text{T}_{\text{high}} = +85^{\circ} \\ & (\text{LM339}) \ \text{T}_{\text{low}} = 0^{\circ}\text{C}, \ \text{T}_{\text{high}} = +70^{\circ}\text{C} \\ & (\text{MC3302}) \ \text{T}_{\text{low}} = -40^{\circ}\text{C}, \ \text{T}_{\text{high}} = +85^{\circ}\text{C} \\ & (\text{LM2901}) \ \text{T}_{\text{low}} = -40^{\circ}\text{C}, \ \text{T}_{\text{high}} = +105^{\circ} \\ & (\text{LM2901V}) \ \text{T}_{\text{low}} = -40^{\circ}\text{C}, \ \text{T}_{\text{high}} = +125^{\circ}\text{C} \\ \end{array}$

- 3. At the output switch point, $V_O \approx 1.4$ Vdc, $R_S \leq 100~\Omega$ 5.0 Vdc $\leq V_{CC} \leq 30$ Vdc, with the inputs over the full common mode range (0 Vdc to V_{CC} –1.5 Vdc).
- 4. The bias current flows out of the inputs due to the PNP input stage. This current is virtually constant, independent of the output state.
- 5. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals, 300 ns is typical.

PERFORMANCE CHARACTERISTICS ($V_{CC} = +5.0 \text{ Vdc}$, $T_A = T_{low} \text{ to } T_{high} \text{ [Note 2.])}$

		LI	M239/33	39	LM2	2901/29	01V		MC3302	2	
Characteristic	Symbol	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
Input Offset Voltage (Note 3.)	V _{IO}	-	_	±9.0	-	-	±15	-	_	±40	mVdc
Input Bias Current (Notes 3., 4.) (Output in Analog Range)	I _{IB}	_	_	400	-	-	500	-	_	1000	nA
Input Offset Current (Note 3.)	I _{IO}	-	-	±150	_	-	±200	_	-	±300	nA
Input Common Mode Voltage Range	V _{ICMR}	0	_	V _{CC} -2.0	0	-	V _{CC} -2.0	0	-	V _{CC} -2.0	V
Saturation Voltage $V_{I}(-) \geq +1.0 \text{ Vdc}, \ V_{I}(+) = 0, \\ I_{sink} \leq 4.0 \text{ mA}$	V _{sat}	_	_	700	_	_	700	_	_	700	mV
Output Leakage Current $V_I(+) \ge +1.0 \text{ Vdc}, V_I(-) = 0,$ $V_O = 30 \text{ Vdc}$	I _{OL}	_	_	1.0	_	_	1.0	_	_	1.0	μА
Differential Input Voltage All V _I ≥ 0 Vdc	V _{ID}	_	_	V _{CC}	_	-	V _{CC}	-	-	V _{CC}	Vdc

- 2. (LM239) T_{low} = -25°C, T_{high} = +85° (LM339) T_{low} = 0°C, T_{high} = +70°C (MC3302) T_{low} = -40°C, T_{high} = +85°C (LM2901) T_{low} = -40°C, T_{high} = +125°C (LM2901V) T_{low} = -40°C, T_{high} = +125°C
- 3. At the output switch point, $V_O \approx 1.4$ Vdc, $R_S \leq 100 \ \Omega$ 5.0 Vdc $\leq V_{CC} \leq 30$ Vdc, with the inputs over the full common mode range (0 Vdc to V_{CC} –1.5 Vdc).
- 4. The bias current flows out of the inputs due to the PNP input stage. This current is virtually constant, independent of the output state.
- 5. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals, 300 ns is typical.

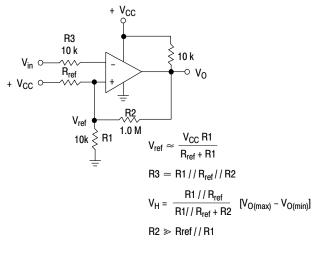


Figure 2. Inverting Comparator with Hystersis

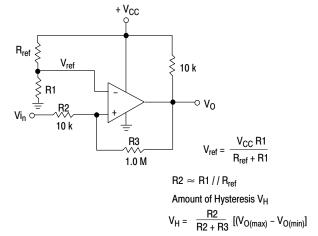
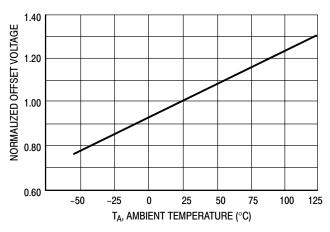


Figure 3. Noninverting Comparator with Hysteresis

Typical Characteristics

 $(V_{CC} = 15 \text{ Vdc}, T_A = +25^{\circ}\text{C} \text{ (each comparator) unless otherwise noted.)}$



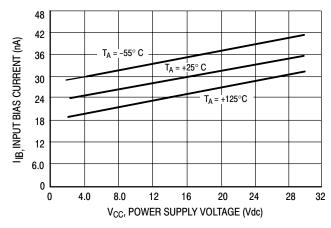


Figure 4. Normalized Input Offset Voltage

Figure 5. Input Bias Current

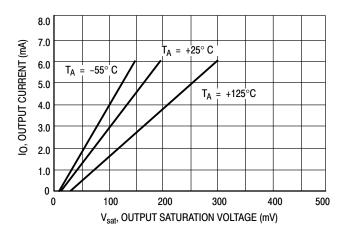
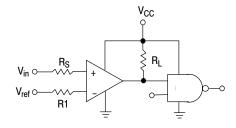


Figure 6. Output Sink Current versus
Output Saturation Voltage



 R_S = Source Resistance $R1 \simeq R_S$

Logic	Device	V _{CC} (V)	R _L kΩ
CMOS	1/4 MC14001	+15	100
TTL	1/4 MC7400	+5.0	10

Figure 7. Driving Logic

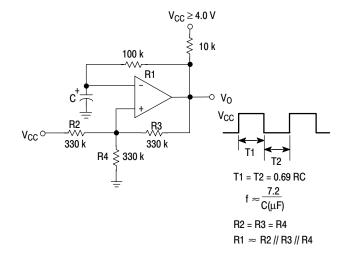


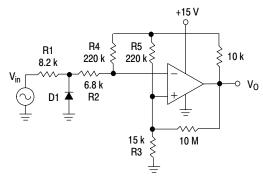
Figure 8. Squarewave Oscillator

APPLICATIONS INFORMATION

These quad comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors < 10 k Ω should be used. The

addition of positive feedback (< 10 mV) is also recommended. It is good design practice to ground all unused input pins.

Differential input voltages may be larger than supply voltages without damaging the comparator's inputs. Voltages more negative than -300 mV should not be used.



D1 prevents input from going negative by more than 0.6 V.

$$R1 + R2 = R3$$

$$R3 \leq \frac{R5}{10} \ \ \text{for small error in zero crossing}$$

Figure 9. Zero Crossing Detector (Single Supply)

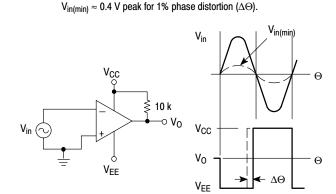


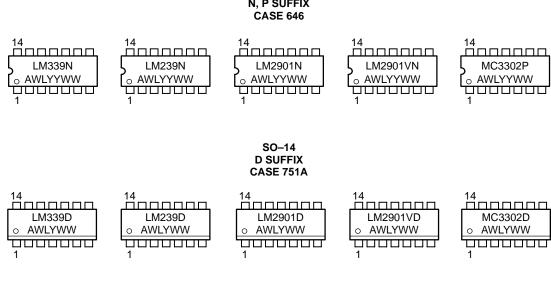
Figure 10. Zero Crossing Detector (Split Supplies)

ORDERING INFORMATION

Device	Package	Shipping	
LM239D	SO-14	55 Units/Rail	
LM239DR2	SO-14	2500 Units/Tape & Reel	
LM239N	PDIP-14	25 Units/Rail	
LM339D	SO-14	55 Units/Rail	
LM339DR2	SO-14	2500 Units/Tape & Reel	
LM339N	PDIP-14	25 Units/Rail	
LM2901D	SO-14	55 Units/Rail	
LM2901DR2	SO-14	2500 Units/Tape & Reel	
LM2901N	PDIP-14	25 Units/Rail	
LM2901VDR2	SO-14	2500 Units/Tape & Reel	
LM2901VN	PDIP-14	25 Units/Rail	
MC3302D	SO-14	55 Units/Rail	
MC3302DR2	SO-14	2500 Units/Tape & Reel	
MC3302P	PDIP-14	25 Units/Rail	

MARKING DIAGRAMS

PDIP-14 N, P SUFFIX

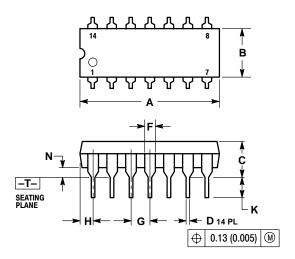


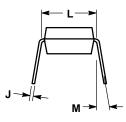
= Assembly Location

WL = Wafer Lot YY, Y = Year

PACKAGE DIMENSIONS

PDIP-14 **P SUFFIX** CASE 646-06 ISSUE M





- NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- Y 14.5M, 1982.

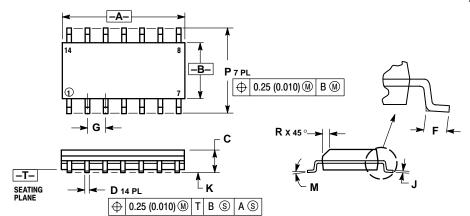
 CONTROLLING DIMENSION: INCH.

 DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.

 DIMENSION B DOES NOT INCLUDE MOLD FLASH.
- 5. ROUNDED CORNERS OPTIONAL.

	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.715	0.770	18.16	18.80	
В	0.240	0.260	6.10	6.60	
С	0.145	0.185	3.69	4.69	
D	0.015	0.021	0.38	0.53	
F	0.040	0.070	1.02	1.78	
G	0.100	BSC	2.54 BSC		
Н	0.052	0.095	1.32	2.41	
7	0.008	0.015	0.20	0.38	
K	0.115	0.135	2.92	3.43	
L	0.290	0.310	7.37	7.87	
M		10°		10°	
N	0.015	0.039	0.38	1.01	

SO-14 **D SUFFIX** CASE 751A-03 ISSUE F



NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- PEH SIDE.

 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	8.55	8.75	0.337	0.344
В	3.80	4.00	0.150	0.157
С	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	BSC	0.050	BSC
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7°	0 °	7°
Р	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

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